



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

117

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/774,573

02/10/2004

Kou Nagata

SON-2924

8504

23353 7590 01/29/2007
RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER

NGUYEN, HIEN N

ART UNIT

PAPER NUMBER

2824

MAIL DATE

DELIVERY MODE

01/29/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Rule 312 Communication	Application No.	Applicant(s)	
	10/774,573	NAGATA ET AL.	
	Examiner	Art Unit	
	Hien N. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 29 December 2005 under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.


c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

Note: The Amendment of Specification and the new Drawing replacement (Figures 12A & 12B) have been approved to be entered


11/19/07
RICHARD T. ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800



Docket No.: SON-2924
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kou NAGATA, et al.

Application No.: 10/774,573

Confirmation No.: 8504

Filed: February 10, 2004

Art Unit: 2824

For: SEMICONDUCTOR MEMORY DEVICE,
REPAIR SEARCH METHOD, AND SELF-
REPAIR METHOD

Examiner: H. N. Nguyen

AMENDMENT UNDER 37 C.F.R. 1.312)

MS Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Prior to issuance of the patent, applicant respectfully requests entry on this amendment under 37 C.F.R. 1.312 for the above-captioned patent application.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Drawings begin on page 3 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 4 of this paper.

An **Appendix** including amended drawing figures is attached following page 4 of this paper.

OK
to enter
HJ
1/16/07

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0001], page 5 with the following:

However, even in the case of an LSI including a BIST circuit, when information of each abnormal bit is taken out to the outside and calculation is performed by an external computer as in a conventional technique described in Patent Document 1, a memory of the external computer has information on normality/abnormality of bits at all addresses. Thus a capacity of the memory is significantly consumed heavily, and also calculation takes much time.

Please replace paragraph [0002], page 17 with the following:

(2) The repair search circuit 30 determines whether either one of the addresses of the inputted X and Y address pair is set as an address to be masked (repaired) (hereinafter referred to as "mask-set"), that is, whether the mask bit 313X or 313Y is "1." When the address is a mask-set address (hereinafter referred to as a "mask address"), the repair search circuit 30 discards the inputted X and Y address pair.

50A

IN

MODE 1

MODE 2

RST

OUT

51

52

53

54

55

Diagram 50B illustrates a second embodiment of the invention. The circuit includes an input terminal IN connected to a switch 54. Switch 54 is controlled by a signal labeled MODE 2. The output of switch 54 is connected to switch 55. Switch 55 is controlled by a signal labeled RST and its other terminal is connected to ground. The output of switch 55 is connected to a buffer 52. The output of buffer 52 is connected to switch 53. Switch 53 is controlled by a signal labeled MODE 1 and its other terminal is connected to ground through a network of capacitors and resistors. The output of switch 53 is connected to an output terminal OUT.